

Description

[THIN FILM TRANSISTOR AND PIXEL STRUCTURE THEREOF]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92121252, filed on August 4, 2003.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] The present invention relates to a structure of a semiconductor device, and more particularly, to a thin film transistor (TFT) and a pixel structure with the thin film transistor.

[0004] Description of the Related Art

[0005] A thin film transistor liquid crystal display is composed of a thin film transistor array substrate, a color filter array substrate and a liquid crystal layer, wherein the thin film transistor array substrate is composed of many thin film transistors arranged in an array and pixel elec-

trodes corresponding to each thin film transistor to form pixel structures. The thin film transistor mentioned above includes a gate electrode, a channel layer, a source region and a drain region which is adapted to serve as a switch for a liquid crystal display element. However, the typical pixel structure has overlap shift issue as shown in FIGS. 1A and 1B.

[0006] FIGS. 1A and 1B are schematic top views of pixel structures without overlap shift and with overlap shift issues in accordance with the prior art respectively. Referring to FIG. 1A, a schematic top view of a pixel structure 100 without overlap shift in accordance with the prior art is shown. The pixel structure 100 comprises a gate electrode 102, a scan line 104, a gate dielectric layer (not shown), a channel layer 106, a source region 108, a drain region 110, a data line 112, a protection layer (not shown) and a pixel electrode 114. The scan line 104 is electrically connected to the gate electrode 102 and formed on a substrate (not shown), wherein the scan line 104 and the gate electrode 102 are formed from a first metal layer. The gate dielectric layer covers the scan line 104 and the gate electrode 102. In addition, the channel layer 106 is formed over the gate dielectric layer formed over the gate

electrode 102, and the source region 108 and the drain region 110 are formed on the gate dielectric layer beside the gate electrode 102. The source region 108 and the drain region 110 partially overlap the channel layer 106, wherein the source region 108 and the drain region 110 are formed using a second metal layer. Moreover, the data line 112 is formed over the gate dielectric layer and electrically connected to the source region 108, wherein the data line 112 is also formed using the second metal layer. The gate electrode 102, the channel layer 106 and source region 108 and the drain region 110 respectively constitutes a thin film transistor 120. The protection layer is formed over the thin film transistor 120, the scan line 104 and the data line 112, wherein the protection layer has a contact 116 to expose the drain region 110. The pixel electrode 114 is electrically connected to the drain region 110 through the contact 116.

[0007] In the pixel structure mentioned above, a parasitic capacitance $C_{gd(a)}$ within the gate electrode 102 and the drain region 110 depends on the overlap area of the gate electrode 102 and the drain region 110. If the parasitic capacitance within the gate electrode 102 and the drain region 110 changes, the performance of a liquid crystal display

will be affected therefrom.

[0008] The main cause of changing the parasitic capacitance within the gate electrode and the drain region results from the misalignment of the first metal layer, i.e. the gate electrode, and the second metal layer, i.e. the source/drain regions, as shown in FIG. B. In comparison with FIG. 1A, the second metal including the data line 112, the source/drain regions 108 and 110, respectively, shown in FIG. 2B shifts; therefore, the parasitic capacitance $C_{gd(a)}$ within the gate electrode 102 and the drain region 110 varies with the overlap area of the gate electrode 102 and the drain region 110 as to generate mura effects.

SUMMARY OF INVENTION

[0009] Therefore, one object of the present invention is to provide a thin film transistor and a pixel structure having the thin film transistor to substantially reduce the variance of the parasitic capacitance within the gate electrode and the drain region. Even though an overlap shift of the gate electrode and the drain region occurs, the parasitic capacitance does not change.

[0010] In accordance with the above object and other advantages, the present invention provides a thin film transistor, comprising a gate electrode having at least one notch,

a gate dielectric layer, a source region, a drain region and a channel layer. The gate electrode is formed on a substrate and the gate dielectric layer is formed over the substrate and covers the gate electrode. The source region is formed on the gate dielectric layer, wherein the source region is over a region outside the notch of the gate electrode and the source region overlaps a portion of the gate electrode. The drain region is formed over the gate dielectric layer exposed by the source region, wherein the drain region is over the notch of the gate electrode and the drain region overlaps a portion of the gate electrode at the edge of the notch. Moreover, the channel layer is formed on the gate dielectric layer formed over the gate electrode and between the source region and drain region.

[0011] In one embodiment, the source region can overlap the gate electrode or be divided into two strip regions, wherein each of the two strip regions adjacent to each longitudinal of the drain region.

[0012] The present invention further provides a pixel structure, comprising a scan line, a data line, a gate electrode, a gate dielectric layer, a channel layer, a source region, a protection layer, a contact and a pixel electrode. The scan line is formed on a substrate. The gate electrode is also

formed on the substrate and electrically connected to the scan line, wherein the gate electrode has at least one notch. The gate dielectric layer is formed over the substrate and covers the scan line and the gate electrode. The channel layer is formed over the gate dielectric layer formed on the gate electrode. The source region is formed on the channel layer, wherein the source region is over a region outside the notch of the gate electrode and the source region overlaps a portion of the gate electrode. The drain region is formed over the channel layer exposed by the source region, wherein the drain region is over the notch of the gate electrode and the drain region overlaps a portion of the gate electrode at the edge of the notch. The data line is formed on the gate dielectric layer and electrically connected to the source region. The protection layer is formed over the substrate and covers the gate electrode, the gate dielectric layer, the channel layer, the source region, the drain region, the scan line and the data line. The contact is formed within the protection layer and electrically connected to the drain region. In addition, the pixel electrode is formed on the protection layer and electrically connected to the drain region through the contact.

[0013] In one embodiment, the source region can overlap the

gate electrode or be divided into to two strip regions, wherein each of the two strip regions adjacent to each longitude of the drain region. Moreover, the source region further extends over the gate dielectric layer formed on the scan line.

[0014] The present invention further provides a thin film transistor, comprising a scan line, a gate electrode, a gate dielectric layer, a channel layer, a drain region and a trident source region. The scan line is formed on a substrate. The gate electrode is formed on the substrate and electrically connected to the scan line, wherein the gate electrode has at least one notch. The gate dielectric layer is formed over the substrate and covers the scan line and the gate electrode. The drain region is formed over the notch of the gate electrode and overlaps a portion of the gate electrode at the edge of the notch and a portion of scan line. The trident source region is formed on the gate dielectric layer, wherein the trident source region comprises: two first projecting portions formed on the gate dielectric layer, wherein the two first projecting portions are over a region outside the notch of the gate electrode and the two first projecting portions overlap a portion of the gate electrode; a second projecting portion formed over the

scan line between the two first projecting portions, wherein the second projecting portion is shorter than the two first projecting portions; and a connection portion, connecting the second projecting portion and the two first projecting portions. In addition, the channel layer formed between the gate electrode and the drain and trident source regions.

[0015] In the structure mentioned above, the connection portion of the trident source region extends over the scan line. In addition, the structure further comprises a data line formed on the gate dielectric layer and electrically connected to the trident source region.

[0016] Because the present invention uses an asymmetric design for the source region and drain region, when an misalignment of the first metal layer, i.e. the gate electrode, and the second metal layer, i.e. the source region and drain region, occurs, the parasitic capacitance $C_{gd(a)}$ does not change severely. In addition, the structure of the source/drain regions in accordance with the present invention can also be applied to a repair structure.

[0017] In order to make the present invention mentioned above, objects, features and advantages thereof or therefrom understandable, a preferred embodiment complying with

configurations is described below in detail.

BRIEF DESCRIPTION OF DRAWINGS

[0018] FIGS. 1A and 1B are schematic top views of pixel structures without overlap shift and with overlap shift issues in accordance with the prior art respectively.

[0019] FIG. 2 is a schematic top view of a pixel structure according to a preferred embodiment of the present invention.

[0020] FIGS. 3A and 3B are enlarged schematic top views of the III region of the thin film transistor of FIG. 2 without overlap shift and with overlap shift issues respectively.

[0021] FIGS. 4A to 4F are schematic cross-sectional configurations along IV–IV of FIG. 3 showing progression steps of a fabrication process of a thin film transistor in accordance with the present invention.

[0022] FIG. 5 and FIG. 6 are schematic top views of exemplary embodiments in accordance with the present invention.

[0023] FIG. 7 is a schematic top view of a thin film transistor according to a preferred embodiment of the present invention.

DETAILED DESCRIPTION

[0024] FIG. 2 is a schematic top view of a pixel structure according to a preferred embodiment of the present invention.

As shown in FIG. 2, the pixel structure 200 comprises a scan line 204, a gate electrode 202, a gate dielectric layer 205, a source region 208, a drain region 210, a channel layer 206, a data line 212, a protection layer (not shown), a contact 216 and a pixel electrode 214. The scan line 204 is formed on a substrate (not shown). The gate electrode 202 is also formed on the substrate and electrically connected to the scan line 204, wherein the gate electrode 202 has at least one notch 203. Moreover, the shape of the notch 203 of the gate electrode 202 can be a triangle, such as an isosceles triangle, a non-isosceles triangle or an equilateral triangle, a quadrilateral, such as a rectangular, a square or a trapezoid, or a non-regular shape and not limited to the shape shown in the figures. The gate dielectric layer 205 is formed over the substrate and covers the scan line 204 and the gate electrode 202. The channel layer 206 is formed over the gate dielectric layer 205 formed on the gate electrode 202. The source region 208 is formed on the channel layer 206, wherein the source region 208 is over a region outside the notch 203 of the gate electrode 202 and the source region 208 overlaps a portion of the gate electrode 202. The drain region 210 is formed over the channel layer 206 exposed by the

source region 208, wherein the drain region 210 is over the notch 203 of the gate electrode 202 and the drain region 208 overlaps a portion of the gate electrode 202 at the edge of the notch 203. Moreover, the channel layer 206, the source region 208, the drain region 210 and the gate electrode 202 constitute a thin film transistor 220. Moreover, an etch stop layer, such as I stopper, is formed between the channel layer 206 and the source and drain regions 208 and 210 respectively. The data line 212 is formed on the gate dielectric layer 205 and electrically connected to the source region 208. The protection layer is formed over the thin film transistor 220, the scan line 204 and the data line 212. The contact 216 is formed within the protection layer and electrically connected to the drain region 210. In addition, the pixel electrode 214 is formed on the protection layer and electrically connected to the drain region 210 through the contact 216. In order to describe the advantages of the present invention in detail, please refer to FIGS 3A and 3B.

[0025] FIGS. 3A and 3B are enlarged schematic top views of the III region of the thin film transistor of FIG. 2 without overlap shift and with overlap shift issues respectively. As shown in FIGS. 3A and 3B, in the thin film transistor 220 of the

present invention the parasitic capacitance $C_{gd(a+b)}$ in which the gate electrode 202 and the drain region 210 do not have overlap shift shown in FIG. 3A, and the parasitic capacitance $C_{gd(a''+b'')}$ in which the gate electrode 202 and the drain region 210 have overlap shift shown in FIG. 3B depends on the overlap area of the gate electrode 202 and the drain region 210. The design of the present invention can substantially reduce the variance of parasitic capacitance; moreover, even if an overlap shift of the gate electrode and the drain region occurs, the parasitic capacitance of the gate electrode 202 and the drain region 210 does not change, wherein the channel layer 206 is represented by a dot region over the gate electrode 202.

[0026] In addition, in some embodiments, the notch 203 of the gate electrode 202 can be extended as to current variance resulting from the overlap variance in horizontal direction.

[0027] FIGS. 4A to 4F are schematic cross-sectional configurations taken along IV–IV of FIG. 3, showing the progression process steps of a fabrication process of a thin film transistor in accordance with the present invention. As shown in FIG. 4A, in the thin film transistor of the embodiment a first metal layer for forming the scan line 204 as shown in FIG. 3A and the gate electrode 202 is formed on a sub–

strate 400. A gate dielectric 402 is then formed over the substrate 400 and covers the scan line and the gate electrode 202. An amorphous silicon (α -Si) layer 404 and an etch stop layer 406 are sequentially formed thereon, wherein the material of the etch stop layer 406 is, for example, silicon nitride.

[0028] Then, Referring to FIG. 4B, a photoresist layer 408 is formed over the substrate 400. A photomask 410 located over the gate electrode 202 is utilized to perform an exposure process 412 for the photoresist layer 408. A region 408c which is exposed during the exposure process is defined as a region that the channel layer 206 as shown in FIG. 3A is going to be formed therein.

[0029] Referring to FIG. 4C, another exposure process 414 is then performed on the photoresist layer 408 from the backside of the substrate 400 in which the exposed region 408b uses the first metal layer, i.e. the gate electrode 202, as a photomask.

[0030] Referring to FIG. 4D, the exposed photoresist layer 408 is developed and the remaining photoresist layer 408c serves as an etch mask for patterning the etch stop layer 406.

[0031] Referring to FIG. 4E, the remaining photoresist layer is re-

moved and an ohmic-contact layer 416 is formed over the substrate 400 and covers the amorphous silicon layer 404 and the etch stop layer 406. Then, a second metal layer 418 is formed on the ohmic-contact layer 416.

[0032] Referring to FIG. 4F, the source region 208 and drain region 210 are formed by patterning the second metal layer 418. From the photomask used for patterning the second metal layer 418, portions of the ohmic-contact layer 416 and the amorphous silicon layer 404 are removed. Because the etch stop layer 406 is formed on a portion of the gate electrode 202, the amorphous silicon layer 404 beneath the etch stop layer 406 is not removed and forms the channel layer 206.

[0033] In addition, the structure of the thin film transistor of the present invention includes some variations as shown in FIG. 5 and FIG. 6.

[0034] FIG. 5 and FIG. 6 are schematic top views of exemplary embodiments in accordance with the present invention. Referring to FIG. 5 and FIG. 6, the structure of the scan line 504 and gate electrode 502 are the same as shown in FIG. 4A. The channel layers 506, i.e. the dot region, as shown in FIG. 5 and FIG. 6 are both formed over the gate dielectric layer 505 formed on the gate electrode 502; the

difference therein is the structures of the source region 508 and the drain region 510. As shown in FIG. 5, the drain region 510 overlaps a portion of the gate electrode 502 at the edge of the notch 503, and the source region 508 includes two strip regions in which each of the two strip regions is adjacent to each longitude of the drain region 510. As shown in FIG. 6, the drain region 510 overlaps a portion of the gate electrode 502 at the edge of the notch 503 and a portion of scan line 504, and the source region 508 includes two strip regions in which each of the two strip regions is adjacent to each longitude of the drain region 510 and extends over the scan line 504.

[0035] In addition, referring to FIG. 7, the structure of the present invention can also be applied to a repair structure.

[0036] FIG. 7 is a schematic top view of a thin film transistor of a preferred embodiment according to the present invention. Referring to FIG. 7, a thin film transistor 700 of the present invention comprises a scan line 704, a gate electrode 702, a gate dielectric layer 705, a channel layer 706, a drain region 710 and a trident source region 708. The structure of FIG. 7 is similar to that of FIG. 4C, wherein the channel layer 706, i.e. the dot region, is on the gate dielectric layer 705 formed on the gate electrode 702. The

difference between FIG. 7 and FIG. 4C is that the trident source region 708 of FIG. 7 is formed on the gate dielectric layer 705, wherein the trident source region comprises: two first projecting portions 708a formed on the gate dielectric layer 705; a second projecting portion 708b formed over the scan line 704 between the two first projecting portions 708a; and a connection portion 708c connecting the second projecting portion 708b and the two first projecting portions 708a. The two first projecting portions 708a are over a region outside the notch 703 of the gate electrode 702 and the two first projecting portions 708a overlap a portion of the gate electrode 702. Moreover, the second projecting portion 708b is shorter than the two first projecting portions and the connection portion 708c can be over the scan line 704. Therefore, when one projecting portion 708a or 708b of the trident source region 708 does not work, the connection between the connection portion 708c and the failed projecting portion can be disconnected for repairing.

[0037] As the described above, a feature of the present invention includes forming an asymmetric structure of the drain region and the source region so that when a misalignment between the first metal layer, i.e. the gate electrode, and

the second metal layer, i.e. the drain region and the source region, occurs, the variance of parasitic capacitance C_{gd} can be substantially reduced. In addition, the source/drain structures of the present invention can also be applied in a repair structure; therefore, the device yield can be improved.

[0038] Although the present invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly to include other variants and embodiments of the invention which may be made by those skilled in the field of this art without departing from the scope and range of equivalents of the invention. Therefore, the scope of the present invention should be interpreted by the claims described below.